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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,715	09/25/2003	David A. Luick	ROC920030293US1	6101

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IBM CORPORATION, INTELLECTUAL PROPERTY LAW
DEPT 917, BLDG. 006-1
3605 HIGHWAY 52 NORTH
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EXAMINER	
ROJAS, MIDYS	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,715	LUICK, DAVID A.	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 9/29/06 have been fully considered but they are not persuasive.

Applicant argues that Dean does not teach the monitoring of the cache miss rates of more than one processor in order to allocate cache lines of more than one private caches to the processors. Instead, Dean discloses a single unified multi-port cache. However, in the system of Dean, if a processor A's miss counter is larger than processor B's miss counter by a predetermined cache reallocation factor, some ways of the cache will be assigned to processor A, wherein cache ways are allocated to each processor so that each group of cache ways represents a particular private cache section for that processor. Therefore, a group of cache ways out of the multi-port cache represents one private cache for each processor. Consequently, the system of Dean does teach more than one private cache, one for each processor, where each private cache is represented in the form of a group of cache ways (abstract).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Dean et al. (6,604,174)

Regarding Claim 1, Dean discloses a method for reducing latencies associated with accessing memory for more than one processors (Proc1 110 to ProcM 112, Figure 1, wherein "processes 110, 111, and 112 can be individual processors...", Col. 4, lines 15-16), each coupled with an associated private cache 130, the method comprising: determining cache miss rates of the more than one processors (cache miss percentage 194, Col. 4, lines 48-58) when issuing cache requests against one or more private caches (hit/miss indications 190 are used to determine the cache miss percentage); comparing the cache miss rates of the more than one processors (each cache miss counter for each processor in system metric 191 is compared to the others, Col. 9, lines 49-62); and allocating cache lines from more than one of the private caches to a processor of the more than one processors based upon the difference between the cache miss rate for the processor and the cache miss rates of other processors ("if a processor A's miss counter is larger than processor B's miss counter by a predetermined cache reallocation factor, some ways of the cache will be assigned to processor A", wherein cache ways are allocated to each processor so that each group of cache ways represents a particular private cache section for that processor).

Claim 5 is rejected using the same rationale as that of Claim 1 wherein the threshold cache miss rate is represented by the predetermined cache reallocation factor 195 (Col. 10, lines 4-10). Additionally, in reallocating the cache ways, cache requests associated with the first processor (processor A) will be forwarded to the way that was previously owned by the second

processor (reallocated way of processor B). The cache lines in the reallocated way will be replaced with those needed by processor A (see Col. 11, line 29 – Col. 12, line 7).

Claim 13 is rejected using the same rationale as that of Claim 5.

Claim 18 is rejected using the same rationale as that of Claim 5.

Claim 28 is rejected using the same rationale as that of Claim 5.

Claim 33 is rejected using the same rationale as that of Claim 5.

Claim 36 is rejected using the same rationale as that of Claim 5.

Regarding Claims 2, 14, 29, Dean discloses the method wherein determining the cache miss rates comprises counting cache misses of each of the more than one processors (hit/miss indications 190 or historical files, Col. 4, lines 24-30).

Regarding Claims 3, 15, 34, Dean discloses the method wherein allocating cache lines comprises forwarding cache requests from the processor to a private cache associated with another processor. In reallocating the cache ways, cache requests associated with the first processor (processor A) will be forwarded to the way that was previously owned by the second processor (reallocated way of processor B). The cache lines in the reallocated way will be replaced with those needed by processor A (see Col. 11, line 29 – Col. 12, line 7).

Regarding Claims 4, 16, 35, Dean discloses the method wherein allocating cache lines comprises selectively allocating cache lines based upon a priority associated with a cache request of the processor (allocation of cache ways, wherein cache ways have many cache lines, is based on the cache miss percentage wherein the processor with the highest cache miss percentage is given priority and assigned new cache ways first, Col. 10, lines 19-40).

Claims 6, 20, is rejected using the same rationale as that of Claim 2 wherein the counting of the cache misses starts as soon as the system boots (since all cache accesses are taken into account when counting the total number of misses) therefore, this must occur after a cold start and warm-up period.

Regarding Claims 7, 37, Dean discloses the method wherein comparing the cache miss rates comprises comparing the cache miss rates, the cache miss rates being associated with more than one processor modules (each cache miss counter for each processor is compared to the others, Col. 9, lines 49-62).

Regarding Claims 8, 21, 38, Dean discloses the method wherein the threshold cache miss rate predetermined cache reallocation factor is based upon an average cache miss rate for the more than one processors (see Col. 10, lines 4-10 and Col. 4, lines 48-58).

Regarding Claims 9-10, 23-24, 32, 39-41, Dean discloses the method wherein forwarding the cache request comprises selecting the second private cache based upon a least recently used cache line associated with the private caches (allocation of cache ways, wherein cache ways have many cache lines, is based on the cache miss percentage wherein the processor with the highest cache miss percentage is given priority and assigned new cache ways first, Col. 10, lines 19-40. This means that the processor with a least recently used way, due to a low cache miss percentage, gives up a cache way to allocate it to the processor with the high miss percentage).

Regarding Claims 11, 17, 25, Dean discloses the method wherein forwarding the cache request comprises selecting the cache request based upon a priority associated with the cache request (LRU algorithm preferentially writes over a process' data when that data is in a way

assigned to a different process, Col. 11, lines 55-67). The LRU information 740 is representative of the least recently cache line table.

Regarding Claims 12, 22, 42, Dean discloses the method wherein forwarding the cache request is responsive to a software instruction that overrides a result of comparing the cache miss rates to forward the cache request to the second private cache (updating of allocation way assignment performed by tag allocation controller 161, see Col. 11, lines 40-55).

Regarding Claim 19, Dean discloses the apparatus wherein the more than one processors (110-112) and the more than one private caches (cache ways allocated to each processor so that each group of cache ways represents a particular private cache section for that processor) reside on more than one processor modules (see Figure 1).

Regarding Claim 26, Dean disclose the apparatus wherein the cache request forwarder (memory controller 160) inserts the cache request into a cache request queue (process to cache multiplexor 120 which holds N output addresses) for the private cache to store the memory line in the private cache (Col. 4, lines 5-23).

Regarding Claim 27, Dean discloses the apparatus wherein the cache request forwarder 160 comprises an arbitrator 161 to arbitrate between the cache request and another cache request from another processor of the more than one processor, to forward the cache request to the cache request queue (Col. 4, lines 59-65).

Regarding Claim 30, Dean discloses the system further comprising a software application to enable the cache request forwarder to forward the cache requests (updating of allocation way assignment performed by tag allocation controller 161, see Col. 11, lines 40-55) based upon the

difference between the number of cache misses associated with the first processor and the number of cache misses associated with the second processor (Col. 9, lines 49-62).

Regarding Claim 31, Dean discloses the system wherein the cache request forwarder allocates cache lines of the first private cache and the second private cache based upon the difference between the cache miss rates of the first processor and the second processor (Col. 9, lines 49-62).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Midys Rojas
Examiner
Art Unit 2185

HONG CHONG KIM
PRIMARY EXAMINER

MR